Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
AUS920030496US1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

Application Number	Filed
10/646,425	08/22/2003

First Named Inventor
Emrah Acar

Art Unit	Examiner
2825	Yelena Rossoshek

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☑ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record.
Registration number 47,573.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Richard F. Frankeny
Signature

Richard F. Frankeny
Typed or printed name

512.370.2872
Telephone number

06/12/2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Emrah Acar et al.	:	Before the Examiner: Yelena Rossoshek
Serial No.: 10/646,425	:	Group Art Unit: 2825
Filed: August 22, 2003	:	Confirmation No. 9656
Title: METHOD FOR DETERMINING AND USING LEAKAGE CURRENT SENSITIVITIES TO OPTIMIZE THE DESIGN OF AN INTEGRATED CIRCUIT	:	IBM Corporation Intellectual Property 11400 Burnet Road Austin, Texas 78758

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

In response to the Final Office Action having a mailing date of April 06, 2006, Applicants respectfully request the formal review of the legal and factual basis of the rejections in this case prior to the filing of an Appeal Brief. A Notice of Appeal is filed concurrently herewith.

REMARKS/ARGUMENTS

Claims 1-20 are pending.

Claims 1-20 are rejected.

I. DRAWINGS

The drawings have been objected to because FIG. 4 and FIG. 5 have errors in labeling. The Applicants have submitted corrected drawing replacement sheets for FIGS. 4 and 5 in a separate Amendment under *37 C.F.R.§ 1.111* filed concurrently herewith.

II REJECTIONS UNDER 35 U.S.C. §102(e)

The Examiner rejects Claims 1-20 under *35 U.S.C.§ 102(e)* as being anticipated by *Cohn et al.* (U.S. Patent 6,711,719). In the Examiner interview of November 22, 2005, the Applicants discussed with the Examiner and the Examiner agreed that this was the incorrect reference. While the Examiner rejects the claims as being anticipated by *Cohn et al.* (U.S. 6,711,719), the Examiner actually uses recitations from *Cohn et al.* (U.S. Patent 6,687,883) (hereinafter "*Cohn*") in the rejection arguments.

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The present invention has 10 claims (Claims 1-10) directed to a method for designing an IC and 10 claims (Claims 11-20) directed to a computer program product that implements the method steps for designing the IC.

Claims 1-10 disclose a method for designing an integrated circuit (IC) having IC parameters including process, circuit, and environmental design parameters comprising a series of 5 design steps. In the "Field of Invention" of *Cohn* cited by the Examiner, *Cohn*

states that his invention relates to a system and method for reducing leakage current in a semiconductor device by providing reduction control circuitry in accordance with probability determination. *Cohn* does not disclose a method for designing an integrated circuit (IC) having IC parameters including process, circuit, and environmental design parameters as recited in Claim 1.

The Applicants assert that *Cohn* only teaches a method and system for inserting leakage control in logic circuits and his method is only used on circuitry that is in a "don't care" state. *Cohn* does not address how the circuitry in an IC is designed to optimize leakage power when the circuits are active. The abstract of *Cohn* succinctly describes his method as the steps of: using (observability) don't care information to identify "sleep states" for individual nets; determining based on probabilistic analysis at least one net in which expected power consumption will be reduced by forcing a net to a particular value during at least a portion of a "sleep state"; and forcing the determined net to the determined value determined portion of that "sleep state." *Cohn* describes his method, in particular step 210 of FIG. 6, as a step forcing a logical change in the net while preserving function.

In the present invention, probabilities of logic states are only used to determine a particular macro's activity to assess total power dissipation. The IC parameters including process, circuit, and environmental design parameters are independent of logic states. The invention of *Cohn* is directed to reducing leakage power to a minimum in circuits that are in a "don't care" condition. When it is known that circuitry is in a don't care state (e.g., standby), *Cohn* can activate his control method to force logic states in the "don't care" circuitry because the forced states are not used in any computation.

Every design modification undertaken by *Cohn* is directed to enabling his inserted control logic to force logic states such that the leakage power of the standby circuitry is minimized. *Cohn* does not modify his circuitry to reduce its intrinsic leakage power when it is in an active state as is recited by the present invention. *Cohn's* sensitivity analysis is directed to each net and determines the sensitivity of leakage power as a

function of state probability of the net. *Cohn* does not determine sensitivity of leakage power to the IC parameters recited in Claim 1. *Cohn* does not mention actual temperature as a parameter as asserted by the Examiner, rather *Cohn* discusses "simulated annealing" as a statistical method using a Boltzmann distribution where " temperature" is a "pseudo variable." The Examiner states that "factoring a gate" is a process parameter where the Applicants could not find a definition of this term in *Cohn* or by searching the internet.

The present invention is directed to a particular method of reducing active leakage power of an IC by making changes during design. The method of *Cohn* would be applied only after leakage power was reduced using the present invention or other method for reducing leakage power when circuitry is active. *Cohn* could take the resulting circuit and determine whether adding additional circuitry for forcing logic states in during partial or total "don't care" periods would result in further leakage reduction.

The Applicants assert that the Examiner has only found descriptive terms in *Cohn* that are similar to terms found in the present invention and then incorrectly concluded that *Cohn* reads on the present invention. The following are a few examples of these failings:

The present invention uses leakage sensitivities of IC parameters including process, circuit, and environmental design parameters to determine which parameters to modify during design to lower leakage. *Cohn* uses sensitivity analysis to make an informed decision of which nets to use adding gates to force logic states in circuitry when in stand-by. The Examiner incorrectly states that *Cohn* use of "simulated annealing" with a pseudo variable called temperature (which is a purely statistical mathematical process) is the same as an environmental parameter of temperature. Further, the Examiner incorrectly states that *Cohn's* "factoring a gate" is a process parameter when the Applicants could not find any description in *Cohn* of what is meant by "factoring a gate".

To anticipate a claimed invention, the reference must disclose the identical invention in as complete detail as is contained in the claim. The Applicants assert that

the Examiner has failed to make a prima facie case of anticipation and has incorrectly applied the invention of *Cohn* in rejecting the claims of the present invention.

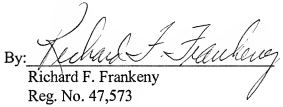
III. CONCLUSION:

The Applicants submit that the rejections of Claims 1-20 under *35 U.S.C.§ 103(a)* as being anticipated by *Cohn* are improper. Applicants respectfully request that this case be reopened and that the rejections be withdrawn and a timely Notice of Allowance be issued.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Patent Agent and Attorney for Applicant

By: 

Richard F. Frankeny
Reg. No. 47,573
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2872

Austin_1 314376v.1